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Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
PAN, DANIEL H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/880,621	Applicant(s) DRYSDALE ET AL.	
	Examiner Daniel Pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-9,13-15,33-36,41-44 and 62-64* is/are allowed.

6)☒ Claim(s) *1-3,10-12,16,20-23,26-28,31,32,37-40,45-58 and 65* is/are rejected.

7)☒ Claim(s) *17-19,24,25,29,30,59-61 and 66-68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/07/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-68 are presented for examination.

2. Claims 25,30 are objected to because of the following informalities. Claims 25 and 30 are believed to be dependent from claims 24, and 29, respectively, because the antecedent basis of the read only and read write registers was found in claims 24,29. It is believed that this is an oversight of applicant, therefore, it is a minor formality of the language. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-3, 10-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Levy et al. (6,092,175).

4. As to claims 1, 3,10,12, since no specific format of the decode is being recited in the claim, the language "decode" is read in view of the specification as the mapping of the system resources. See the table mapping the physical register pairs of the given thread in page 7 of applicant's specification. Levy disclosed a multithreaded system (see fig.5D, see also figs 5C for the first thread and second thread) comprising at least :

a) a first processing entity (fist thread);

b) a second processing entity (second thread);

c) using a first register (see any shared register in the register pool) to communicate a first processing entity and second entity ;

d) using a second register (see any other shared register in the register pool) to communicate a first processing entity and second entity

d)a plurality of registers (see fig.5D) to allow communication between the first processing entity and second processing entity, wherein eh plurality of registers are cross decoded by the first entity and second entity (see any of the registers can be allocated to any of the threads in col.10, lines 42-52, see also col.10, lines 5-17 for the renaming registers shared across the threads, see also the mapping in the renaming table in col.9, lines 22-32 for the background teaching of mapping).

5. It is "cross decoded" because any one of the shared registers can be allocated to any of the threads based on the mapping (col.10, lines 42-60).

6. As to claims 2,11, Levy's thread was also a core because it was directed to group of programs (see col.1, lines 26-27).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Torii (6,330,661).

8. As to claim 16, Torii disclosed a system (see fig.1) including at least :

a) fist core based on firmware (1-0);

b) second core firmware (1-1);

c) hardware based communication mechanism [physical common register file] to allow communication between the first core and second core such that the firs core and second core can execute identical code paths (see the identical structures of thread execution unit 0 and thread execution unit 1 in fig.1) to communicate each other. AS to the firmware see the multithreaded microprocessor executing instructions in col.1, lines 10-14 for background).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 20-23,28, 37-39 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Torii (5,913,059).

10. As to claims 20,23,28,37, Torii disclosed a processing system including at least :

a) a plurality of processing entities, or threads (see fig.9 [21a][21b], see the parallel processing of the threads in cool.8, lines 34-42) having associated with a first register [27a] to enable one of the processing entities (see 21a) to receive information (information from arithmetic result unit #1 in 21b, see fig.10) relating to anther processing entity (21b) , and a second register [24a] to enable the processing entity

[21a] to output information for use by another proceeding entity [21b] (see information outputted to register selector unit # 1 in fig.11);

b) logic circuit [26a] or means to apply a logic operation (selection) to at least contents of the second register [24a][24b] of each of the processing entities (see output lines from the 24a in the entity 21a and from 24 b in entity 21b) and store, or means for storing a result of the logic operation (see direct output from 26a, and indirect output through AU28a) in first register [27a] [27b] of each processing entity (see the result form selector 26a and the result further processed by arithmetic 28a and stored into 27b of other processing entity 21b in fig.9, col.9, lines 42-50, see also col.10, lines 14-42 for the operation of selector 26a and 26 b).

11. Since no specific chain of a result of the logic operation is being recited in the claim, the language "a result of the logic operation" is being read as any result derived from the selector output, either the direct output from the selector (output of 27a), or indirect output t from the selector through the Arithmetic Unit 28a).

12. As to claims 21, 38, Torii's entities were processing cores (see fig.9, 21a21b).

13. As to claim 22, 39, Torii's processing entities were directed to threads (e.g. see tow thread parallel processors in col.8, lines 34-42).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 26,27,31,32, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Torii (5,913,059) in view of Delaruelle et al. (5,095,523).

15. As to claims 26,27,31,32, 40, the limitations of parent claims 23, 28, 37 have been discussed in paragraph # 10 , therefore, it will not be repeated herein. Torii did not specifically show his logic circuit was programmable and perform bit wise operation as claimed. However, Delaruelle disclosed a system including a programmable logic circuit for performing bit wise operation (e.g. see fig.1, col.1, lines 51-64, for summary, see fig.4, col.2, lines 50-64, col.3, lines 60-68, col.4, lines 1-6 for details). It would have been obvious to one of ordinary skill in the art to use Delaruelle in Torii for including programmable circuit as claimed because the use of Delaruelle could provide the control ability of Torii to adapt to specific selection of the logic options at a predetermined set of command from the user, and it could be achieved by configuring the programmable logic circuit of Delaruelle into Torii with modified read/write ports such that the programmable logic of Delaruelle could be recognized by Torii in order ton achieve the flexible control over the logic operations by the programming, and in doing so , provided a motivation.

16.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claim 45-58 are rejected under 35 U.S.C. 102(a) (b) as being anticipated by Schimmel (6,496,909)

18. As to claim 45, 53, 56, 58, Schimmel taught (see fig.s4, see also fig.5 for hardware structure) :

a) first core (see the thread for requesting the access in col.9, lines 29-35);

b) second core (see the additional competing threads);

c) a register (shared by the threads) which included a bit [lock bit] used to synchronize the operation of the first and second cores (see the requesting thread determining lock bit for the access with other threads in col.9, lines 29-46, see also fig.5 entries of memory table storing the lock bit in col.10, lines 25-41).

19. As to claim 58, additional bits of the first register [lock bits] and second register [waits] were also applicable in Schimmel without additional memory space (see col.9, lines 11-15).

20. As to claim 46, 54, Schimmel also taght a second register [wait bit] used to synchronize the operation of a first core [requesting thread] and a second core (the competing threads), wherein the first core was configured to execute a predetermined synchronization instruction by setting the bit in the first register [lock bit] to a value and then waiting until the bit in the second register [wait bit] was set before proceeding (e.g. see fig.4 410 414 416 418 420, see execution of the thread after the wait bit set [416] based on the setting of lock bit [410] in col.9, lines 30-56, see fig.4).

21. As to claim 47, 57, see the activation of additional selected thread (second core) in the wait queue (fig.4 [422] [424][426]).

22. As to claim 48,55, the first register [lock bit] and second register [wait bit] were cross decoded because it were bit patterns in table entries recognizable by the competing cores (competing threads, see the table entries for the wait bit and lock bit in col.10, lines 28-40).

23. As to claim 49, Schimmel also included a core (see fig.5 [[500]) to execute a first thread and second thread (see the competing threads in col.9, lines 29-56);
b)) a register which included a bit [lock bit] used to synchronize the operation of the first and second cores (see the requesting thread determining lock bit for the access with other threads in col.9, lines 29-46, see also fig.5 entries of memory table storing the lock bit in col.10, lines 25-41).

24. As to claim 50 , Schimmel also taght a second register [wait bit] used to synchronize the operation of a first core [requesting thread] and a second core (the competing threads), wherein the first core was configured to execute a predetermined synchronization instruction by setting the bit in the first register [lock bit] to a value and then waiting until the bit in the second register [wait bit] was set before proceeding (e.g. see fig.4 410 414 416 418 420, see execution of the thread after the wait bit set [416] based on the setting of lock bit [410] in col.9, lines 30-56, see fig.4).

25. As to claim 51, see the activation of additional selected thread (second core) in the wait queue (fig.4 [422] [424][426]).

As to claim 52, the first register [lock bit] and second register [wait bit] were cross decoded because it were bit patterns in table entries recognizable by the competing cores (competing threads, see the table entries for the wait bit and lock bit in col.10, lines 28-40).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claim 65 rejected under 35 U.S.C. 103(a) as being unpatentable over Manabe (5,590,326) in view of Wong et al. (5,909,695).

27. As to claim 65, the word "communicate" is read as communication of information either directly or indirectly, and/or both. Manabe taught at least :

a) a first register [520 lock set up unit] to communicate information from a first processing [50 left] to a second processing entity [50 right] (see fig.2);

b) a second register [520 lock set up unit] to communicate information from the second processing entity [50 right] to the first processing entity [50 left];

c) means for cross decoding the first register and second register between the first processing entity [5o left] and second processing entity [50 right].

28. Manabe did not specifically show the shared cache as claimed. However, Wong disclosed a system including a shared cache (e.g. see col.1, lines 40-44, col.5, lines 2-

8, lines 15-44). It would have been obvious to one of ordinary skill in the art o use Wong in Manabe for including the shared cache as claimed because the use of Wong could provide the capability of Manabe to accept the data by the processing threads at a predetermined common format in a shorter cycle based on the smaller memory structure, such as cache, thereby increasing the efficiency of the memory access, and because Manabe did disclose a shared memory unit [40] which would have been recognized by one of ordinary skill in the art to implement the sharable characteristic of the memory unit in a cache memory, which had already been known for its efficiency in speed , and since there is no specific cache access or structural format of the cache being recited in the claim, therefore, any known type of cache, such as taught by Wong, in the art should be applicable in a sharable manner into Manabe, and for the above reasons , provided a motivation.

29. As to the RAM and ROM, Wong also taught RAM and ROM (see fig.1).

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Borkenhagen et al. (6,567,839) is cited for the background teaching of the thread switching logic and the state registers (e.g see col.12, lines 31-67, col.13, lines 1-27).

31. Claims 4-9 , 13-15 are allowable over the art of record for reciting the combined features of the first register decoded by first thread (or core) to have first register name and decoded by the first thread to have second register name, and the second register decoded by the first thread to have the second register name and decoded by the second thread (or core) to have the first register name.

32. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims None of the prior art of record further teaches the combined features of the first resister decode by the first core to have first register name and decoded by the second core to have second register name, and the second register decoded by the first core to have the second register name and decoded by the second core to have the first register name.

33. Claims 24-25 , 29,30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the first register being read-only register and the second register being read-write register as claimed.

34. Clams 33-36 are allowable over the art of record for reciting the combined features of the read only register to receive information from other processing core and read write register for outputting information to another processor core and the logical

circuit to apply logic operation on the contents of the read-write register of each cores and store result in the read only register of each core.

35. Claims 41-44 are allowable over the art of record for reciting eh combined features of read only register , read write register and the logic circuitry for apply logic operation on the read register of each cores and store result in each read only register on each cores.

36. Claims 59-61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the information of first register communicated only from the first register to fist core and the information of second register communicated only from the second core to the first core.

37. Clams 62-64 are allowable over the art of record for reciting the combined features of the first register communicating information form the first entity to second entity , the second register for communicating ht information from the second entity to the first entity, the means for cross decoding the first register and second register, the means causing the first entity to set the predetermined bit in the first register, and the means for causing the first processing entity to wait until the corresponding bit in the second register is set before proceeding..

38. Claims 66-68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. None of the prior art of record further teaches the first register communicate information only from the first core to the second core, and the second register communicate information only from the second core to the first core.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP